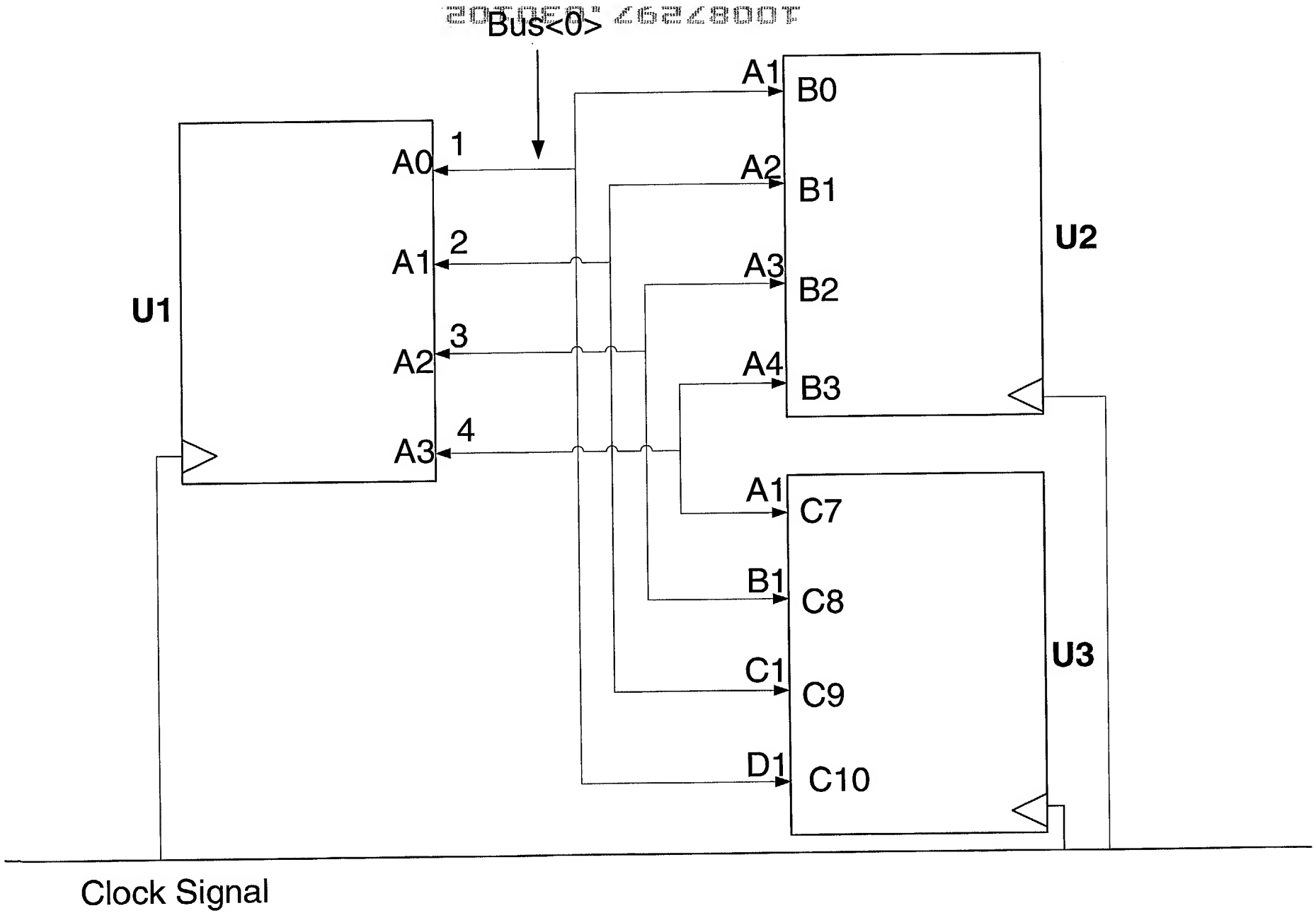


Figure 1
(Prior Art)

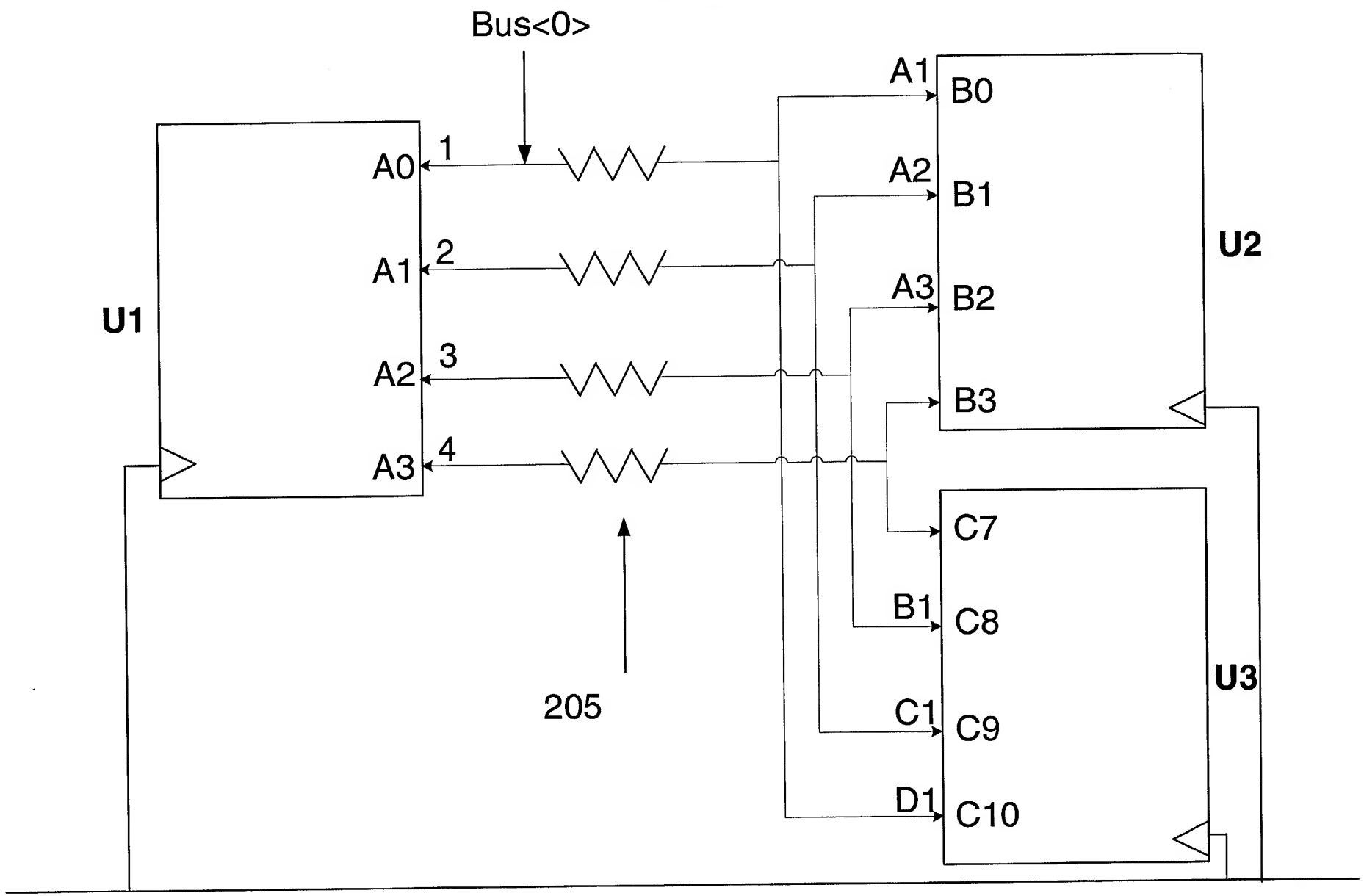
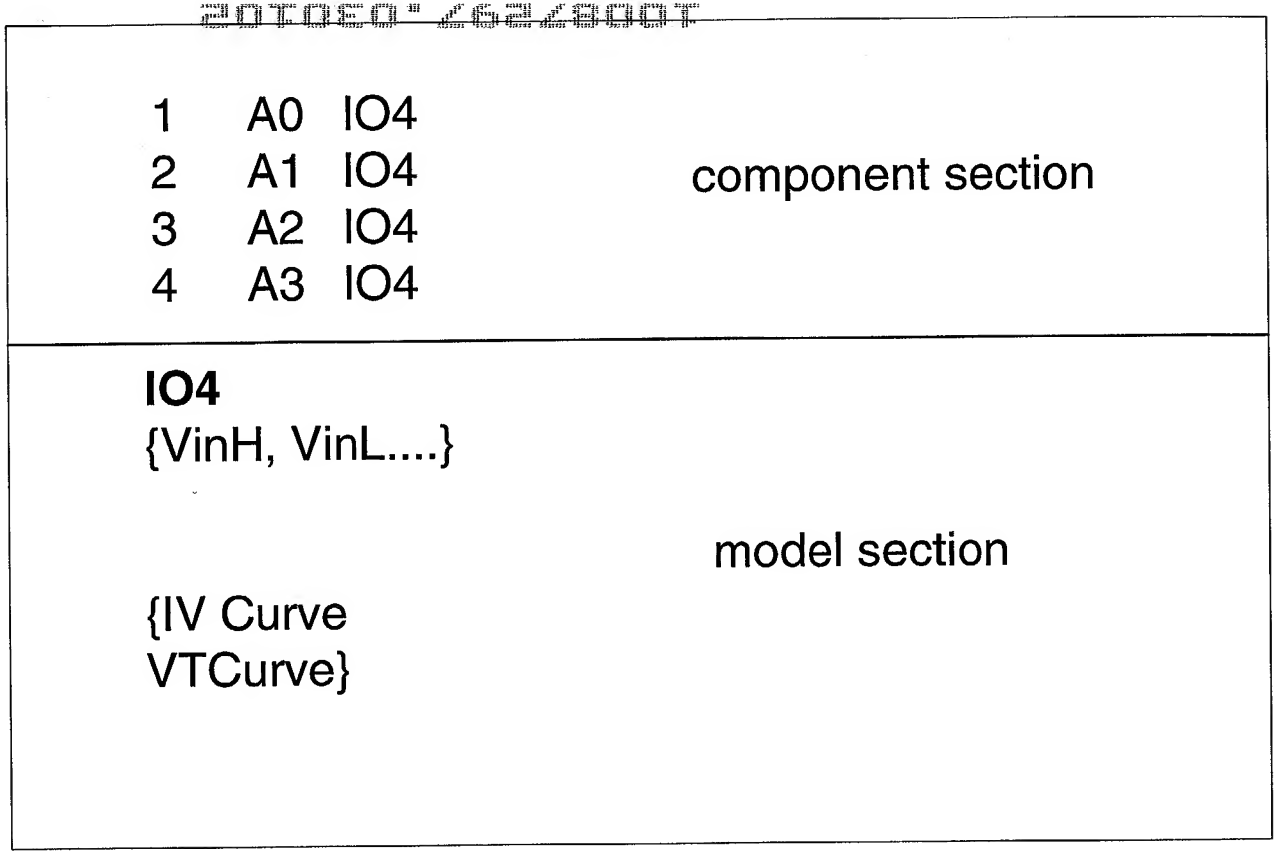


Figure 2
(Prior Art)

Figure 4
(Prior Art)



400

Figure 3 (Prior Art)

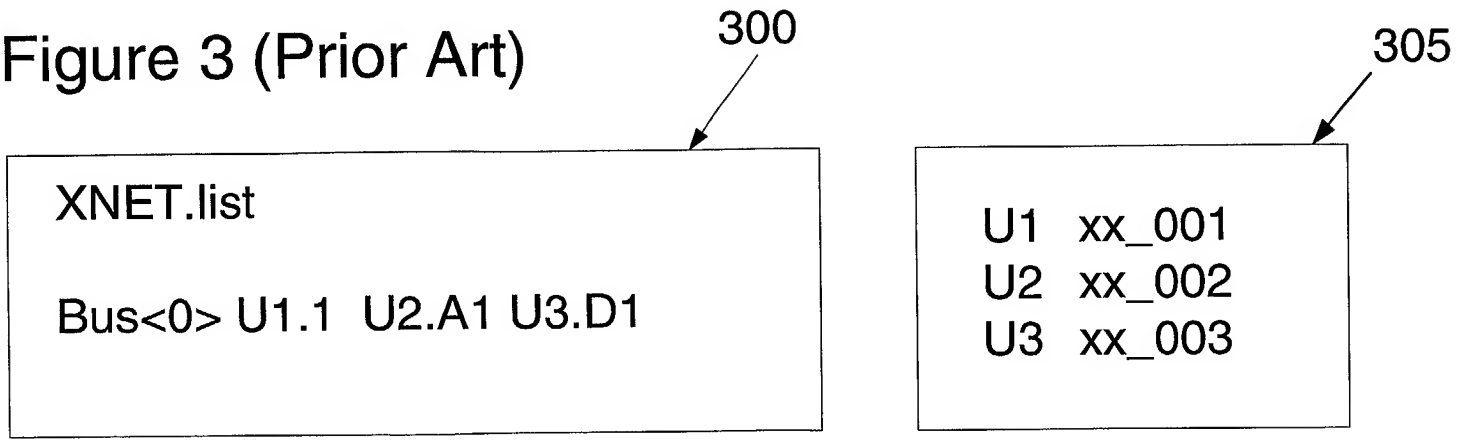


Figure 5

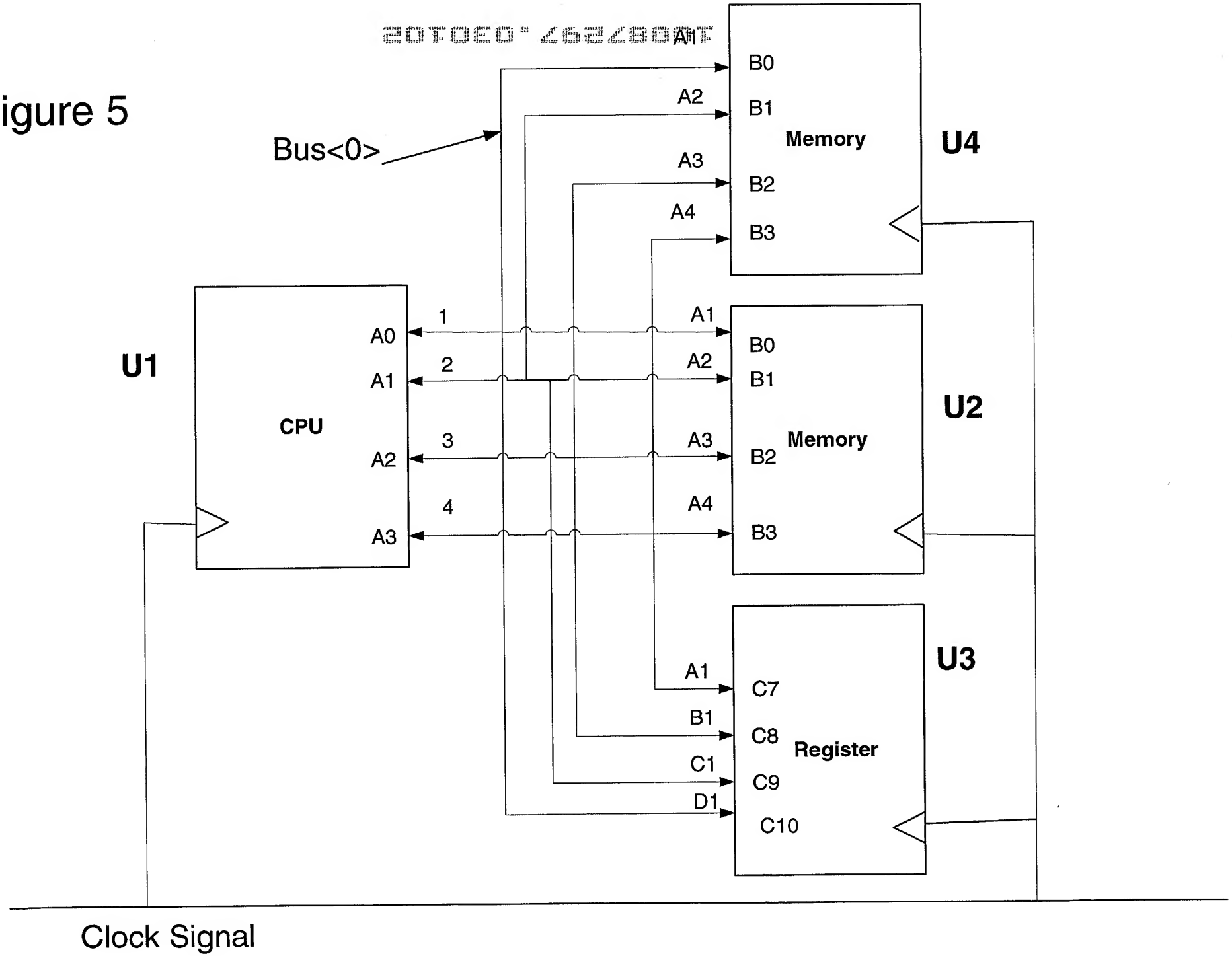

Bus<0>
U1
CPU
A0
A1
A2
A3
1
2
3
4
U4
Memory
B0
B1
B2
B3
A1
A2
A3
A4
U2
Memory
B0
B1
B2
B3
A1
A2
A3
A4
U3
Register
C7
C8
C9
C10
A1
B1
C1
D1
Clock Signal

Figure 6

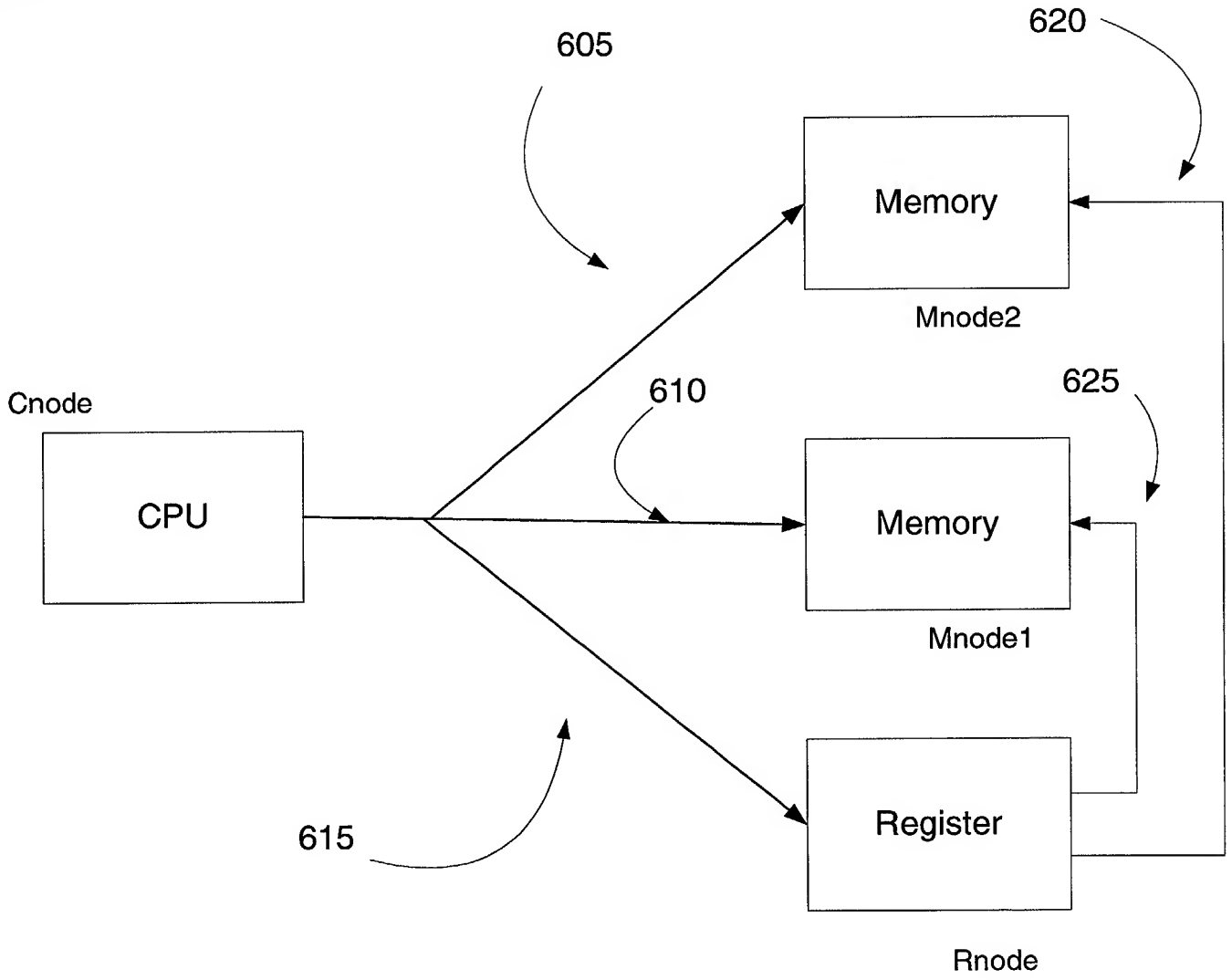

605
620
Memory
Mnode2
Cnode
610
625
CPU
Memory
Mnode1
615
Register
Rnode

Fig. 7A

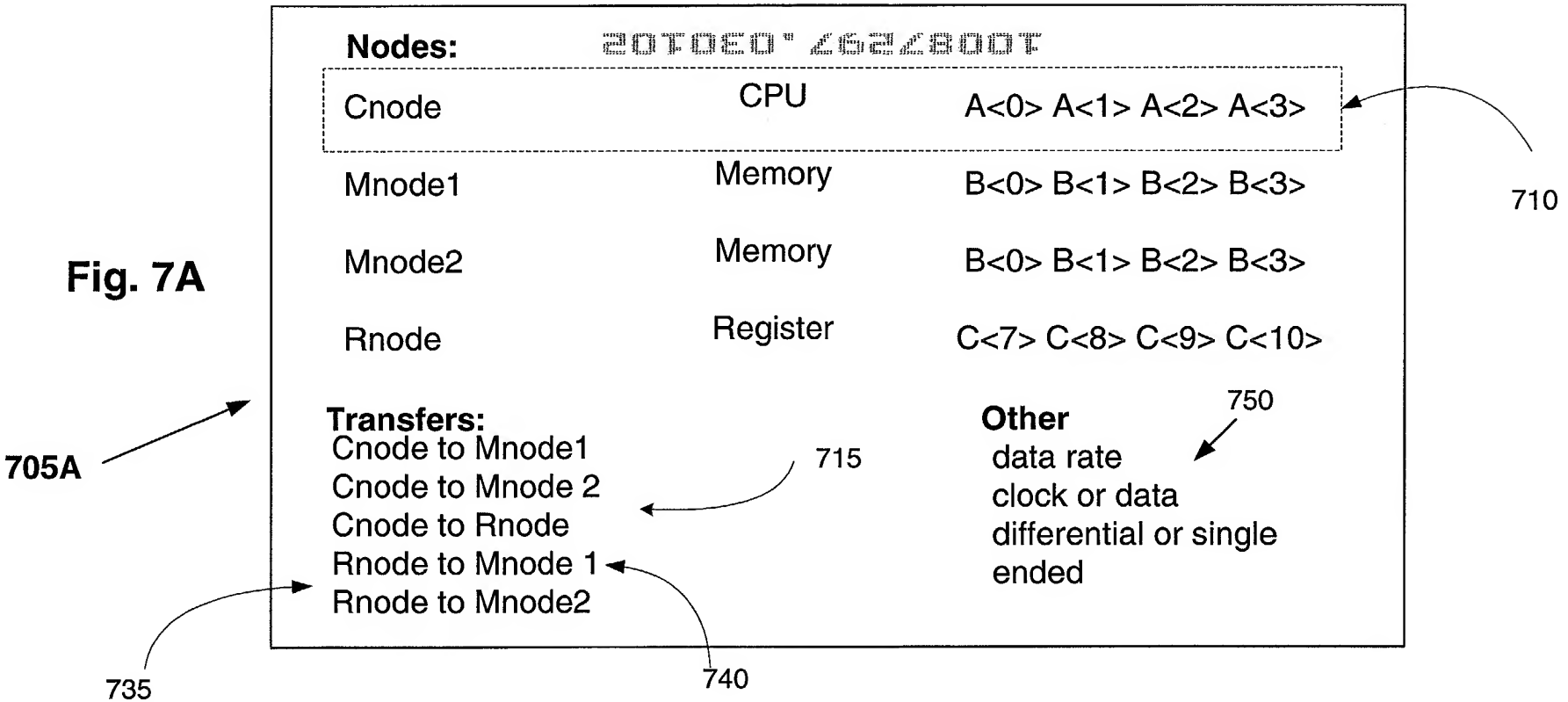

Nodes:
Cnode
CPU
A<0> A<1> A<2> A<3>
Mnode1
Memory
B<0> B<1> B<2> B<3>
Mnode2
Memory
B<0> B<1> B<2> B<3>
Rnode
Register
C<7> C<8> C<9> C<10>
710
705A
Transfers:
Cnode to Mnode1
Cnode to Mnode 2
Cnode to Rnode
Rnode to Mnode 1
Rnode to Mnode2
715
735
740
Other
data rate
clock or data
differential or single ended
750

Fig. 7B

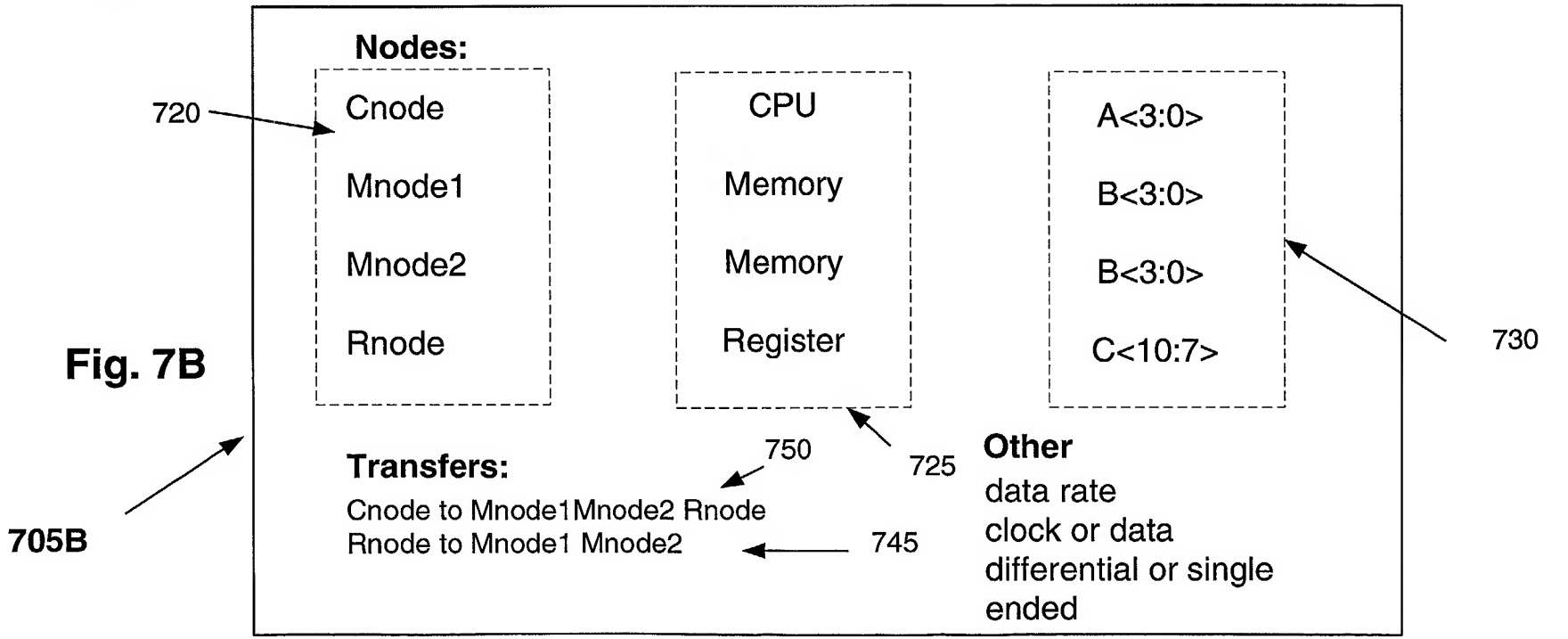

Nodes:
720
Cnode
Mnode1
Mnode2
Rnode
CPU
Memory
Memory
Register
A<3:0>
B<3:0>
B<3:0>
C<10:7>
730
705B
Transfers:
Cnode to Mnode1Mnode2 Rnode
Rnode to Mnode1 Mnode2
745
750
725
Other
data rate
clock or data
differential or single ended

Figure 8

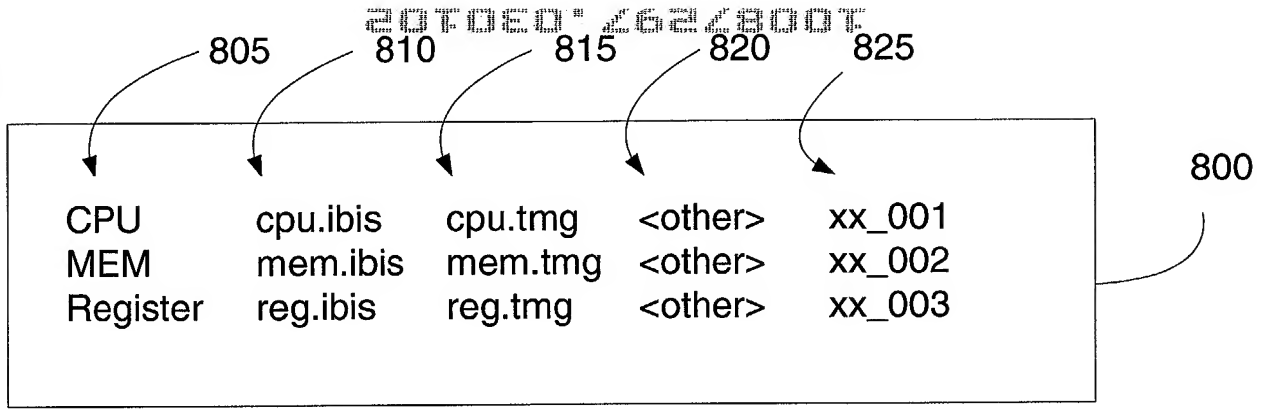


Figure 9

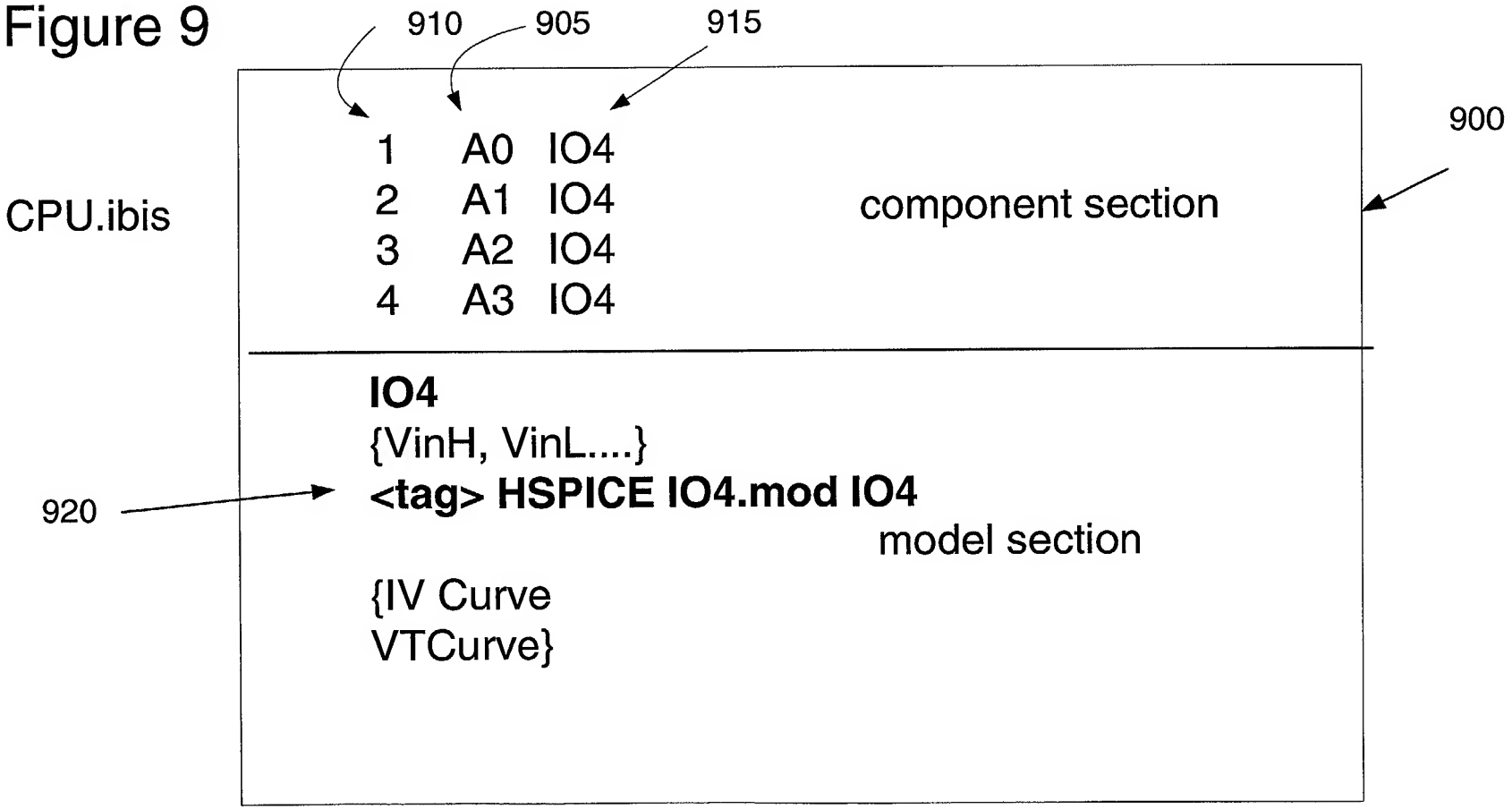
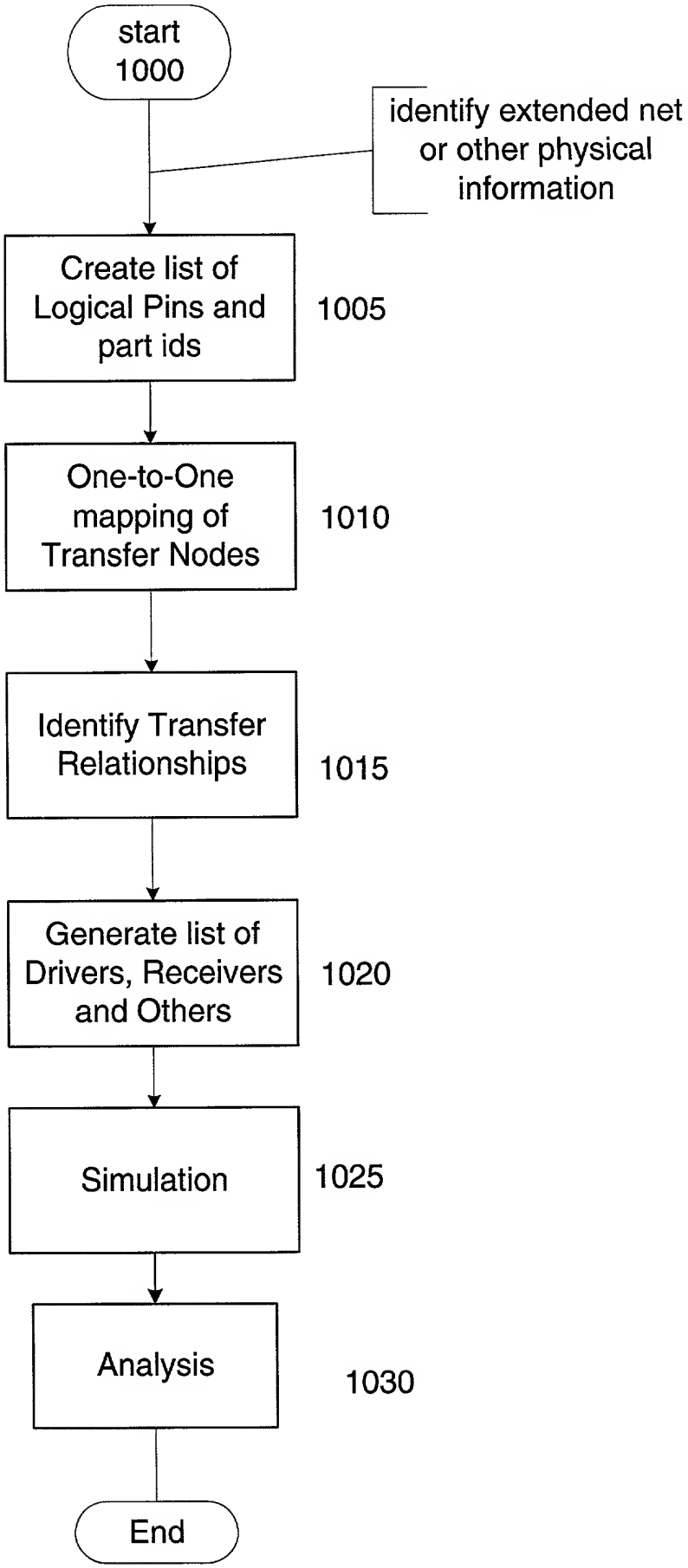


Figure 10



20040207.0306/26997001

Figure 11

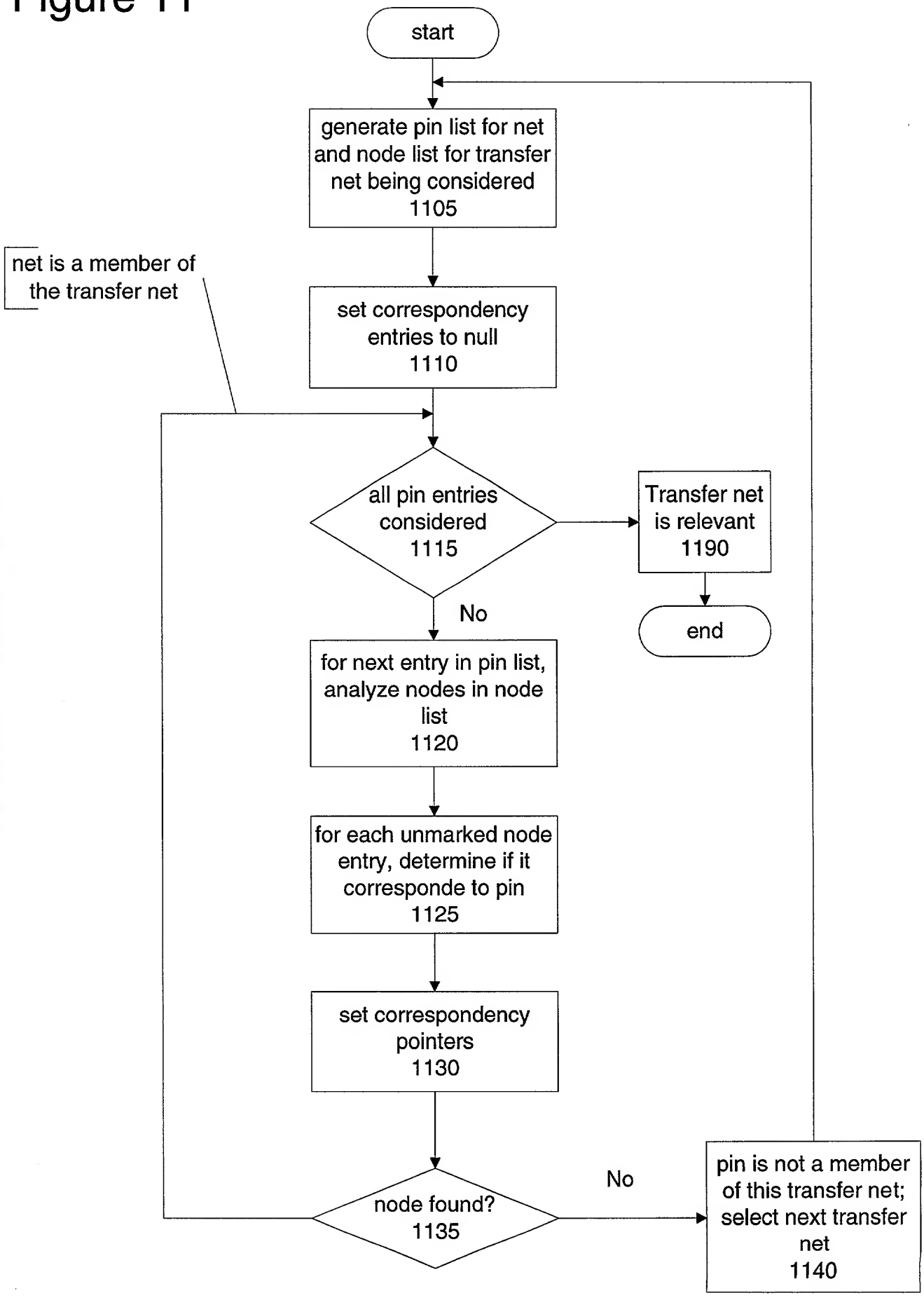
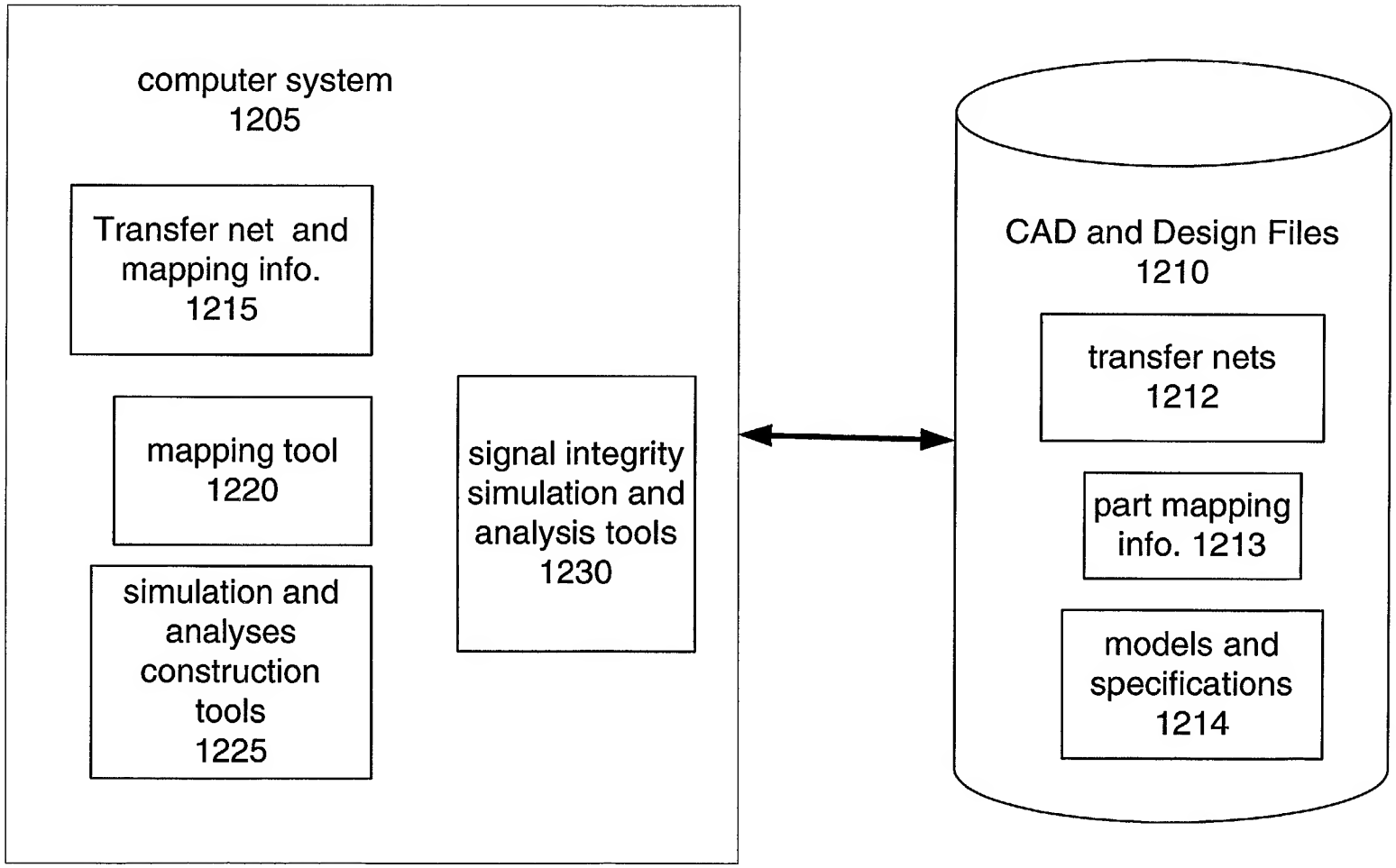

start
generate pin list for net and node list for transfer net being considered 1105
net is a member of the transfer net
set correspondency entries to null 1110
all pin entries considered 1115
Transfer net is relevant 1190
end
No
for next entry in pin list, analyze nodes in node list 1120
for each unmarked node entry, determine if it corresponde to pin 1125
set correspondency pointers 1130
node found? 1135
No
pin is not a member of this transfer net; select next transfer net 1140

Figure 12


computer system
1205
Transfer net and mapping info.
1215
mapping tool
1220
simulation and analyses construction tools
1225
signal integrity simulation and analysis tools
1230
CAD and Design Files
1210
transfer nets
1212
part mapping info. 1213
models and specifications
1214